

SPEECH CODER/DECODER

CROSS-REFERENCE TO RELATED APPLICATIONS:

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BACKGROUND OF THE INVENTION

The present invention relates to a speech
coder/decoder for high quality coding speech signal
5 with designated parameters.

As a usual controllable bit rate speech
coder/decoder, a CDMA (Code Division Multiple
Access) system is well known in the art. This
system is disclosed in, for instance, "Enhanced
10 Variable Rate Coded Speech Service Option 3 for Wide
and Spread Spectrum Digital Systems",
Standardization Recommendation Specifications,
IS-127, TIA TR45 (Literature 1).

In this system, CELP (code excited linear
15 prediction) coding system control parameters are set
from a table, which is produced in advance from
results of bit rate determination on the basis of
input signal features, and the input signal is coded
on the basis of the control parameters set in this
20 way. This system also has a function of forcibly
setting a bit rate on the basis of an external
signal.

This type of speech coder/decoder will now be
briefly described with reference to Fig. 11. In the
25 illustrated speech coder/decoder, the bit rate is
controlled on the basis of an external signal.

The illustrated speech coder/decoder comprises
a speech coder and a speech decoder. The speech

coder and speech decoder include respective coding parameter controllers 51 and 55. In the speech coder, a bit rate is given to the coding parameter controller 51. The coding parameter controller 51
5 selects control parameters corresponding to the given bit rate with reference to a table (not shown, but for instance a ROM (read only memory) with bit rate addresses), in which a plurality of control parameters for controlling the operation of a CELP
10 coder 52 are stored, and provides the selected control parameters to the CELP coder 52. The control parameters are sub-frame length as a unit of excitation signal coding in CELP coding, and bit distribution.

15 An input signal (i.e., input speech signal) is supplied to a CELP coder 52. The CELP coder 52 computes linear prediction coefficients, which represent a spectral envelope characteristic of the input signal, by linear prediction analysis thereof
20 for each predetermined frame. The CELP coder 52 also generates an excitation signal by driving a linear prediction synthesis filter corresponding to the spectral envelope characteristic, and codes the excitation signal on the basis of the bit
25 distribution. The excitation signal is coded for each of a plurality of sub-frames, into which each frame is divided.

The excitation signal noted above is

constituted by a periodic component representing the pitch period of the input signal, a residue signal, and gains of these components. The periodic component representing the pitch period of the input
5 signal, is expressed as an adaptive codevector stored in a codebook called adaptive codebook. The residue component is expressed as a multi-pulse signal, which is disclosed in, for instance, J-P. Adoul et al, "Fast CELP Coding Based on Algebraic
10 Coders" , Proc. ICASSP, pp. 1957-1960, 1987 (Literature 2). The excitation signal is generated by weight imparting the adaptive codevector and the multi-pulse signal by gain data stored in a gain codebook and adding together the results of the
15 weight imparting. A reproduced signal can be synthesized by driving the linear prediction synthesis filter on the basis of the excitation signal.

The selection of the adaptive codevector,
20 multi-pulse signal and gain is controlled such as to minimize error power as a result of acoustical weight imparting of an error signal, which represents an error between the reproduced signal and the input signal. The CELP coder 52 outputs
25 indexes corresponding to the adaptive codevector, multi-pulse signal and gain, and an index representing the linear prediction coefficients, to a multiplexer 53.

The multiplexer 53 provides a bit stream which is obtained by converting the indexes corresponding to the adaptive codevector, multi-pulse signal, gain index and linear prediction coefficients for each frame. Data representing the bit rate is stored in a bit stream header.

In the speech decoder, a multiplexer 54 receives the bit stream, extracts bit stream header data representing the bit rate, and provides the extracted bit rate data to the coding parameter controller 55. Then, the multiplexer 54 extracts the indexes corresponding to the adaptive codevector, multi-pulse signal, gain and linear prediction coefficients from the bit stream for each frame, and provides the extracted data to a CELP decoder 56.

The coding parameter controller 55 executes a similar process to that in the coding parameter controller 51, then selects the control parameters on the basis of the supplied bit rate data, and provides the selected control parameters to the CELP decoder 56.

The CELP decoder 56 executes a decoding process using the indexes corresponding to the adaptive codevector, multi-pulse signal, gain and linear prediction coefficients as well as the sub-frame length and bit rate data. The excitation signal is obtained by weight imparting the adaptive codevector

and multi-pulse signal with gain data held in the gain codebook and adding together the results of the weight imparting. In the CELP decoder 56, the reproduced signal is obtained by driving the linear prediction synthesis filter on the basis of the excitation signal.

As shown above, in the CELP coding system the bit rate is controlled by controlling the sub-frame length as a unit of excitation signal coding and the bit distribution.

In the prior art speech coder/decoder, however, the frame length as a unit of coding is fixed. Therefore, it is impossible to control coding delay, which is defined as time from the instant when a first input signal sample is supplied till the instant of start of the coding.

In addition, in the prior art coder/decoder it is necessary to provide in advance parameters which are necessary for generating the multi-pulse signal. Therefore, the system can serve its function only when a predetermined bit rate is given.

SUMMARY OF THE INVENTION

An object of the present invention therefore is to provide a speech coder comprising a speech coding means for determining an input speech signal excitation signal expressed in the form of a plurality of pulses such as to minimize the distortion, with respect to the input speech signal,

of a reproduced speech signal obtained by exciting a linear prediction synthesis filter, which is prescribed by linear prediction coefficients of the input speech signal, on the basis of the excitation
5 signal, and a control circuit for generating control parameters on the basis of designated control data, the speech coding means serving to code the input speech signal on the basis of the control parameters.

10 According another aspect of the present invention, there is provided a speech coder comprising a speech coding means for determining an input speech signal excitation signal expressed in the form of a plurality of pulses such as to
15 minimize the distortion, with respect to the input speech signal, of a reproduced speech signal obtained by exciting a linear prediction synthesis filter, which is prescribed by linear prediction coefficients of the input speech signal, on the
20 basis of the excitation signal, and a control circuit for receiving a designated bit rate and a coding delay as control data and generating control parameters on the basis of the control data, the speech coding means serving to code the input speech
25 signal on the basis of the control parameters.

According to other aspect of the present invention, there is provided a speech coder comprising a speech coding means for determining an

input speech signal excitation signal expressed in the form of a multi-pulse signal constituted by a plurality of pulses such as to minimize the distortion, with respect to the input speech signal, of a reproduced speech signal obtained by exciting a linear prediction synthesis filter, which is prescribed by linear prediction coefficients of such input speech signal, on the basis of the excitation signal, a control circuit, supplied with the designated bit rate and coding delay as control data, for generating control parameters on the basis of the control data, the speech coding means serving to code the input speech signal on the basis of the control parameters, a control circuit for receiving a designated bit rate and a coding delay as control data and generating control parameters on the basis of the control data, the speech coding means serving to code the input speech signal on the basis of the control parameters, and a parameter setting circuit for setting parameters necessary from coding the multi-pulse signal as setting parameters on the basis of predetermined ones of the control parameters, the predetermined control parameters being supplied to the parameter setting circuits, the speech coding means serving to code the input speech signal on the basis of the control parameters and the setting parameters.

According to an aspect of the present invention

there is provided a speech coder comprising a speech coding means for determining an input speech signal excitation signal expressed in the form of a plurality of pulses such as to minimize the distortion, with respect to the input speech signal, of a reproduced speech signal obtained by exciting a linear prediction synthesis filter, which is prescribed by linear prediction coefficients of the input speech signal, on the basis of the excitation signal, and a control circuit for receiving a designated bit rate, a coding delay and a computational effort extent as control data and generating control parameters on the basis of the control data, the speech coding means serving to code the input speech signal on the basis of the control parameters.

According another aspect of the present invention, there is provided a speech coder comprising a speech coding means for determining an input speech signal excitation signal expressed in the form of a multi-pulse signal constituted by a plurality of pulses such as to minimize the distortion, with respect to the input speech signal, of a reproduced speech signal obtained by exciting a linear prediction synthesis filter, which is prescribed by linear prediction coefficients of such input speech signal, on the basis of the excitation signal, a control circuit, supplied with the

designated bit rate, coding delay and computation amounts as control data, for generating control parameters on the basis of the control data, the speech coding means serving to code the input speech
5 signal on the basis of the control parameters, a control circuit for receiving a designated bit rate and a coding delay as control data and generating control parameters on the basis of the control data, the speech coding means serving to code the input
10 speech signal on the basis of the control parameters, and a parameter setting circuit for setting parameters necessary from coding the multi-pulse signal as setting parameters on the basis of predetermined ones of the control
15 parameters, the predetermined control parameters being supplied to the parameter setting circuits, the speech coding means serving to code the input speech signal on the basis of the control parameters and the setting parameters.

20 According to other aspect of the present invention, there is provided a speech decoder for restoring a reproduced speech signal from received coded speech data, the coded speech data including a speech signal excitation signal, linear prediction
25 synthesis filter coefficients and control data, comprising a control circuit for generating control parameters on the basis of the control data, and speech decoding means for restoring a reproduced

speech signal by restoring the excitation signal and the linear prediction synthesis filter coefficient by decoding from the coded speech data on the basis of the control parameters and exciting a linear prediction synthesis filter, which is prescribed by the linear prediction synthesis filter coefficient, on the basis of the excitation signal.

According to further aspect of the present invention, there is provided a speech decoder for restoring a reproduced speech signal from received coded speech data, the coded speech data including a speech signal excitation signal, linear prediction synthesis filter coefficients, bit rate and coding delay, comprising a control circuit for generating control parameters on the basis of the bit rate and coding delay, and speech decoding means for restoring a reproduced speech signal by restoring the excitation signal and the linear prediction synthesis filter coefficient by decoding from the coded speech data on the basis of the control parameters and exciting a linear prediction synthesis filter, which is prescribed by the linear prediction synthesis filter coefficient, on the basis of the excitation signal.

According still further aspect of the present invention, there is provided a speech decoder for restoring a reproduced speech signal from received coded speech data, the coded speech data including a

speech signal excitation signal, linear prediction
synthesis filter coefficients, a bit rate and a
coding delay, the excitation signal being expressed
in the form of a multi-pulse constituted by a
5 plurality of pulses, the speech decoder comprising a
control circuit for generating control parameters on
the basis of the bit rate and the coding delay, a
parameter setting circuit for setting parameters
necessary for coding the multi-pulse as setting
10 parameters on the basis of predetermine ones of the
control parameters, and speech decoding means for
restoring a reproduced speech signal by restoring
the excitation signal and the linear prediction
synthesis filter coefficient by decoding from the
15 coded speech data on the basis of the control
parameters and the setting parameters and exciting a
linear prediction synthesis filter, which is
prescribed by the linear prediction synthesis filter
coefficient, on the basis of the excitation signal.

20 According to the present invention, there is
provided a speech coding method comprising of
computing frame length from bit rate and coding
delay, selecting control parameters from a table in
which a plurality of control parameters for
25 controlling an operation of CELP coding on the basis
of the bit rate, computing pulse number of
multi-pulse excitation signal, pulse position
candidates of each pulse and candidate positions

thereof from the sub-frame length and bit number of multi-pulse signal.

According to other aspect of the present invention, there is provided a speech coding method
5 comprising dividing an input speech signal into frames on the basis of a given frame length, generating control parameters of frame length, sub-frame length and bit distribution that are necessary for coding, from given bit rate and coding
10 delay data, and setting parameters necessary for generating a multi-pulse signal from the given bit rate and coding delay.

In the present invention, the speech coder comprises a coding parameter control circuit for
15 generating control parameters, i.e., frame length, sub-frame length and bit distribution that are necessary for the coding, from given bit rate and coding delay data. The input speech signal is divided into frames on the basis of the given frame
20 length. A multi-pulse signal coding parameter setting circuit sets parameters, which are necessary for generating a multi-pulse signal from the given bit rate and coding delay.

Since the coding parameter control circuits
25 generates the frame length, sub-frame length and bit distribution data, and the input speech signal is divided into frames on the basis of the generated frame length, it is possible to vary the frame

length which is a unit of processing for the coding.
It is thus possible to control the coding delay in
addition to the bit rate.

Since the multi-pulse signal coding parameter
5 setting circuit sets parameters necessary for the
multi-pulse signal generation, it is possible to
increase the bit rate range. That is, it is not
necessary to set a bit rate in advance.

Other objects and features will be clarified
10 from the following description with reference to
attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram of a speech
coder/decoder according to a first embodiment of the
15 present invention;

Fig. 2 is a block diagram for explaining the
CELP coding circuit shown in Fig. 1;

Fig. 3 is a block diagram for explaining the
CELP decoding circuit shown in Fig. 1;

20 Fig. 4 is a block diagram of a speech
coder/decoder according to a second embodiment of
the present invention;

Fig. 5 is a block diagram for explaining the
CELP coding circuit shown in Fig. 4;

25 Fig. 6 is a block diagram for explaining the
CELP decoding circuit shown in Fig. 4;

Fig. 7 is a block diagram of a speech
coder/decoder according to a third embodiment of the

present invention;

Fig. 8 is a block diagram for explaining the CELP coding circuit shown in Fig. 7;

Fig. 9 is a block diagram of a speech
5 coder/decoder according to a fourth embodiment of the present invention;

Fig. 10 is a block diagram for explaining the CELP coding circuit shown in Fig. 9; and

Fig. 11 is a block diagram of a prior art
10 speech coder/decoder.

PREFERRED EMBODIMENTS OF THE INVENTION

Referring to Fig. 1, a speech coder/decoder is shown, which comprises a speech coder and a speech decoder. The speech coder includes a coding
15 parameter control circuit 11, a CELP coding circuit 12 and a multiplexer 13. The speech decoder includes a demultiplexer 14, a coding parameter control circuit 15 and a CELP decoding circuit 16.

In the speech coder, bit rate and coding delay
20 are given as control data to the coding parameter control circuit 11. The coding parameter control circuit 11 calculates a frame length by subtracting an advance read length, which is necessary for an analytic processing in CELP coding, from the given
25 bit rate and coding delay. For example, in a case where the coding delay is 25 ms and the advance read length of the linear prediction analysis is 5 ms, the frame length is 20 ms.

The coding parameter control circuit 11 selects, on the basis of the given bit rate, control parameters from a table, in which a plurality of control parameters for controlling the operation of the CELP coding circuit 12 are set on the basis of calculated frame length, and provides the selected control parameters to the CELP coding circuit 12. The selected control parameters are frame length, sub-frame length (of 5 ms, for instance) and bit distribution. The CELP coding circuit 12 codes the input signal (input speech signal) on the basis of frame length, sub-frame length and bit distribution that have been set.

The operation of the CELP coding circuit 12 will now be described by having reference also to Fig. 2.

The frame length F that has been set in the coding parameter control circuit 11, is supplied through an input terminal 213 to a frame dividing circuit 201 and a linear prediction coefficient quantizing circuit 204.

The sub-frame length S that has also been set in the coding parameter control circuit 11, is supplied through an input terminal 214 to a sub-frame dividing circuit 202, a linear prediction analysis circuit 203, the linear prediction coefficient quantizing circuit 204, an acoustical weight imparting signal generating circuit 205, an

acoustical weight imparted reproduced signal
generating circuit 206, a target signal generating
circuit 208, an adaptive codebook retrieving circuit
209, a multi-pulse retrieving circuit 210 and a gain
5 retrieving circuit 211.

The bit distribution to the parameters having
been set in the coding parameter control circuit 11,
is supplied through an input terminal 215 to the
linear prediction coefficient quantizing circuit
10 204, adaptive codebook retrieving circuit 209,
multi-pulse retrieving circuit 210 and gain
retrieving circuit 211.

The frame dividing circuit 201 divides the
input signal on the basis of the frame length F
15 having been set, and provides each frame of input
signal to the sub-frame dividing circuit 202.

The sub-frame dividing circuit 202 divides each
frame on the basis of the sub-frame length S having
been set, and provides each sub-frame of input
20 signal to the linear prediction analysis circuit 203
and acoustical weight imparting signal providing
circuit 205.

The linear prediction analysis circuit 203
executes linear prediction analysis of signal
25 (sub-frame signal) provided from the sub-frame
dividing circuit 202 on the basis of the sub-frame
length S having been set for each sub-frame, and
provides linear prediction coefficients $a(i)$ ($i = 1,$

..., N_p) to the linear prediction coefficient quantizing circuit 204, acoustical weight imparting signal providing circuit 205, acoustical weight imparted reproduced signal generating circuit 206,
5 adaptive codebook retrieving circuit 209 and multi-pulse retrieving circuit 210. N_p is the degree number of the linear prediction analysis, for instance 10. The linear prediction analysis may be a self-correlation process or a covariance process,
10 and is detailed in Furui, "Digital Speech Processing", Tokai University Publishing Association (Literature 3).

The linear prediction coefficient quantizing circuit 204 executes collective quantization of the
15 linear prediction coefficients obtained for the individual sub-frames on the basis of the frame length F and sub-frame length S having been set for each frame. In order to reduce the bit rate, this quantization is executed for only the last sub-frame
20 in the frame and using interpolated values of the quantized values of the pertinent and immediately preceding frames as the quantized values of the other sub-frames. This quantization and interpolation are executed after conversion of the
25 linear prediction coefficient into corresponding line spectrum pair (LSP). The conversion of the linear prediction coefficient into LSP is described in, for instance, Sugamura et al, "Speech Data

Compression in Linear Spectrum Pair (LSP) Speech Analysis Synthesis Systems", The Transactions of Institute of Electronics and Communication Engineers of Japan, J64-A, pp. 599-606, 1981 (Literature 4).

- 5 The LSP quantization may be executed in a well-known manner; for instance, it is disclosed in Japanese Laid-Open Patent Publication No. 4-171500 (Literature 5), and it is not described here. The linear prediction coefficient quantizing circuit 204
- 10 converts the quantized LSP into corresponding linear prediction coefficients, and provides the result as quantized linear prediction coefficient $a'(i)$ ($i = 1, \dots, N_p$) to the acoustical weight imparting signal providing circuit 205, acoustical weight
- 15 imparted reproduced signal generating circuit 206, an adaptive codebook retrieving circuit 209 and multi-pulse retrieving circuit 210.

An index representing the quantized LSP is supplied through an output terminal 216 to the

20 multiplexer 13. Linear prediction synthesis filter $H_s(z)$ is expressed by formula (1).

$$H_s(z) = \frac{1}{1 - \sum_{i=1}^{N_p} a'(i)z^{-i}} \quad (1)$$

25

In the acoustical weight imparting signal generating circuit 205, an acoustical weight imparting filter $H_w(z)$ expressed by formula (2) is

formed using the linear prediction coefficients, and is driven by sub-frame input signal to generate an acoustical weight imparted signal. This acoustical weight imparted signal is provided to the target
5 signal generating circuit 208.

$$Hw(z) = \frac{1 - \sum_{i=1}^{Np} a(i)R2^i z^{-i}}{1 - \sum_{i=1}^{Np} a(i)R1^i z^{-i}} \quad (2)$$

10

where R1 and R2 are weight imparting coefficients to control the extent of the acoustical weight imparting and, for instance, R1 = 0.6 and R2 = 0.9.

15 The acoustical weight imparted reproduced signal generating circuit 206 drives the linear prediction synthesis filter and the acoustical weight imparting synthesis filter of the preceding frame with the excitation signal of the preceding
20 sub-frame which is obtained through a sub-frame buffer 207, and provides data representing the states of the two filters after the driving to the target signal generating circuit 208.

The target signal generating circuit 208
25 receives the data representing the states of the linear prediction synthesis filter and acoustical weight imparting filter from the acoustical weight imparting reproduced signal generating circuit 206,

generates a zero input response of a filter which is constituted by the two filters connected in cascade, subtracts the zero input response thus generated from the acoustical weight imparted signal, and provides the resultant difference as the target signal to the adaptive codebook retrieving circuit 209 and multi-pulse retrieving circuit 210 as well as to a gain retrieving circuit 211.

The adaptive codebook retrieving circuit 209 updates a codebook, called adaptive codebook and holding past excitation signals, on the basis of the excitation signal of the immediately preceding sub-frame that is obtained through the sub-frame buffer 207, and then selects an adaptive codevector corresponding to pitch d from the adaptive codebook. When the pitch d is shorter than the sub-frame length, an adaptive codevector is formed by repeatedly connecting excitation signal segments each corresponding to delay d , separated one after another from past excitation signal stored in the adaptive codebook, until reaching of the sub-frame length. The reproduced signal $SAd(n)$ is formed by driving the linear prediction synthesis filter and acoustical weight imparting filter in zero states thereof with the adaptive codevector $Ad(n)$ thus formed, and selects pitch d which minimizes the error E_d between the target signal $X(n)$ and the reproduced signal $SAd(n)$, given by formula (3).

$$Ed = \sum_{n=1}^L X^2(n) - \frac{(\sum_{n=1}^L X(n)SAd(n))^2}{\sum_{n=1}^L SAd^2(n)} \quad (3)$$

5 where L is the sub-frame length set by the coding
parameter control circuit 11. The adaptive codebook
retrieving circuit 209 further provides the selected
pitch d through the output terminal 216 to the
multiplexer 13, and also provides the selected
10 adaptive codevector Ad(n) and the reproduced signal
SAd(n) thereof to the gain retrieving circuit 211.
The adaptive codebook retrieving circuit 209
provides the reproduced signal SAd(n) to the gain
retrieving circuit 211 and provides the reproduced
15 signal SAd(n) to the multi-pulse retrieving circuit
210.

The multi-pulse retrieving circuit 210 forms a
multi-pulse signal constituted by a plurality of
non-zero pulses. The position of each pulse is
20 selected from a plurality of pulse position
candidates predetermined for each pulse. Each pulse
is a polarity pulse. For example, in 8-kHz sampling
with a sub-frame length of 5 ms (i.e., with a sample
number N of 40), the multi-pulse excitation signal
25 is constituted by P (for instance 5) pulses. The
position of each of the P pulses is selected from
M(p) (p = 1, ..., P-1, for instance 8) pulse
position candidates. The multi-pulse retrieving

circuit 210 is holding a plurality of combinations of pulse number P and M(p) pulse position candidates, and selects a combination of pulse number P and M(p) pulse position candidates on the basis of a bit distribution designated by a coding parameter control circuit 11. The multi-pulse retrieving circuit 210 also forms multi-pulse signal Cj(n) by using the selected pulse number P (equal to the number of channels) and M pulse position candidates of each channel, and selects a multi-pulse signal Cj(n) which minimizes formula (4).

$$Ej = \sum_{n=1}^L X'^2(n) - \frac{(\sum_{n=1}^L X'(n)SCj(n))^2}{\sum_{n=1}^L SCj^2(n)} \quad (4)$$

where X'(n) is a subtracted signal of the reproduced signal SA(n) of the adaptive codevector from the target signal X(n) and given by formula (5).

$$X'(n) = X(n) - \frac{\sum_{n=1}^L X(n)SAd(n)}{\sum_{n=1}^L SAd^2(n)} SAd(n) \quad (5)$$

Formula (4) can be minimized with reducing the computational effort extent, for instance by using method as described in Japanese Patent Application No. 7-318071 (Literature 6). The multi-pulse

retrieving circuit 210 provides the selected multi-pulse signal $C_j(n)$ and reproduced signal $SC_j(n)$ thereof to the gain retrieving circuit 211, and provides corresponding index j through the
5 output terminal 216 to the multiplexer 13.

The gain retrieving circuit 211 quantizes the gains G_A and G_C by using the reproduced signal $SAd(n)$ of the adaptive codevector, reproduced signal $SC_j(n)$ of the multi-pulse signal and target signal
10 $X(n)$ such as to minimize formula (6).

$$E_k = \sum_{n=1}^L (X(n) - G_k(1)SAd(n) - G_k(2)SC_j(n))^2 \quad (6)$$

The gain retrieving circuit 211 further forms
15 an excitation signal by using the quantized gain, adaptive codevector and multi-pulse signal, provides the excitation signal thus formed through the sub-frame buffer 207 to the acoustical weight imparted reproduced signal generating circuit 206
20 and adaptive codebook retrieving circuit 209, and an index corresponding to the gain through the output terminal 216 to the multiplexer 13.

Referring now back to Fig. 1, the multiplexer 13 provides a bit stream obtained by conversion from
25 the indexes representing the quantized LSP, pitch, multi-pulse signal and quantized gains for each signal. The bit rate and coding delay data are provided in a header of the bit stream.

In the speech decoder, the bit stream is supplied to the demultiplexer 14. The demultiplexer 14 provides the bit rate and coding delay data present in the bit stream header to the coding parameter control circuit 15, and then it extracts the indexes of the quantized LSP, pitch, multi-pulse signal and quantized gains from the bit stream for each frame, and provides them to the CELP decoding circuit 16.

10 The coding parameter control circuit 15 executes an operation similar to that in the coder side coding parameter control circuit 11; i.e., it selects control parameters on the basis of the input bit rate and coding delay data, and provides the
15 selected control parameters to the CELP decoding circuit 16.

The operation of the CELP decoding circuit will now be described by having reference also to Fig. 3.

The indexes representing the quantized LSP,
20 pitch, multi-pulse signal and quantized gains, are supplied through an input terminal 227 to a linear prediction coefficient decoding circuit 221, an adaptive codebook decoding circuit 222, a multi-pulse signal decoding circuit 223 and a gain
25 decoding circuit 224.

The frame length data set by the coding parameter control circuit 15 is supplied through an input terminal 228 to the linear prediction

coefficient decoding circuit 221 and a frame unifying circuit 226.

5 The sub-frame length data set by the coding parameter control circuit 15 is supplied through an input terminal 229 to the linear prediction coefficient decoding circuit 221, adaptive codebook decoding circuit 222, multi-pulse signal decoding circuit 223 and gain decoding circuit 224 and also to a reproduced signal synthesizing circuit 225 and
10 the frame unifying circuit 226.

The bit distribution data set by the coding parameter control circuit 15 is supplied through an input terminal 230 to the linear prediction coefficient decoding circuit 221, adaptive codebook
15 decoding circuit 222, multi-pulse signal decoding circuit 223 and gain decoding circuit 224.

The linear prediction coefficient decoding circuit 221 receives the index representing the quantized LSP for each frame, and provides quantized
20 linear prediction coefficient $a'(i)$ ($i = 1, \dots, N_p$) restored by decoding for each sub-frame to the reproduced signal synthesizing circuit 225.

The adaptive codebook decoding circuit 222 restores the adaptive codevector by decoding from
25 the pitch data supplied for each sub-frame. The multi-pulse decoding circuit 223 provides the multi-pulse signal restored by decoding from the indexes supplied for each sub-frame to the gain

decoder 224.

The gain decoding circuit 224 restores the gains by decoding from the indexes supplied for each sub-frame, forms an excitation signal by using the
5 adaptive codevector, multi-pulse signal and gains, and provides the excitation signal thus formed to the reproduced signal synthesizing circuit 225.

The reproduced signal synthesizing circuit 225 forms a reproduced signal by driving the linear
10 prediction synthesis filter $H_s(z)$ with the excitation signal for each sub-frame, and provides the reproduced signal thus formed to the frame unifying circuit 226. The linear prediction synthesis filter $H_s(z)$ is expressed by formula (1)
15 noted above. The frame unifying circuit 226 connects together successively supplied sub-frame reproduced signals for the frame length, and provides the resultant reproduced signal for each frame.

20 A different embodiment of the speech coder/decoder according to the present invention will now be described with reference to Fig. 4.

The illustrated coder/decoder comprises a speech coder and a speech decoder. The speech coder
25 includes a coding parameter control circuit 31, a CELP coding circuit 32, a multi-pulse signal coding parameter setting circuit 33 and a multiplexer 13. The speech decoder includes a demultiplexer 14, a

coding parameter setting circuit 34, a CELP decoding circuit 35 and a multi-pulse signal coding parameter setting circuit 16.

In the speech coder, the coding parameter control circuit 31 receives the bit rate and coding delay as control data, and calculates the frame length by subtracting advance read length, which is necessary for an analysis process in CELP coding, from the given bit rate and coding delay. On the basis of the calculated frame length, the coding parameter control circuit 31 selects control parameters from a table, in which a plurality of control parameters for controlling the operation of the CELP coding circuit 32 are stored, on the basis of the supplied bit rate, and provides the selected control parameters to the CELP coding circuit 32. The coding parameter control circuit 31 further provides the bit number distributed to the sub-frame length and multi-pulse signal to the multi-pulse signal coding parameter setting circuit 33.

The multi-pulse signal coding parameter setting circuit 33 computes pulse number P , pulse position candidate number $M(p)$ of each pulse and position candidates thereof, necessary for the multi-pulse excitation signal coding, from supplied sub-frame length N and bit number Y of the multi-pulse signal. The pulse position candidates of each pulse are set such that a sequence of $0, 2, 3, \dots, N-1$ is

interleaved with the pulse number P, as disclosed in Literature 2 noted above. For example, in a case where the sub-frame length is set to 40 (i.e., a sample number N of 40) and the bit number Y of the multi-pulse signal is set to 20, the pulse number P is 5 and the pulse position candidate number M(p) is 8. An example of pulse position candidates in this case is shown in Table 1 below.

$$Y = \sum_{p=0}^{P-1} (1 + \log_2 M(p)) \quad (7)$$

$$N = \sum_{p=0}^{P-1} M(p) \quad (8)$$

TABLE 1

| PULSE No. | PULSE POSITION CANDIDATES |
|-----------|------------------------------|
| 0 | 0, 5, 10, 15, 20, 25, 30, 35 |
| 1 | 1, 6, 11, 16, 21, 26, 31, 36 |
| 2 | 2, 7, 12, 17, 22, 27, 32, 37 |
| 3 | 3, 8, 13, 18, 23, 28, 33, 38 |
| 4 | 4, 9, 14, 19, 24, 29, 34, 39 |

The CELP coding circuit 32 codes the input signal on the basis of the frame length, sub-frame length and bit distribution that are set by the coding parameter control circuit 31, and also the pulse number P, pulse position candidate number M(p) of each pulse and position candidates thereof that are set by the multi-pulse signal coding parameter setting circuit 33.

The operation of the CELP coding circuit 32 will now be described with reference to Fig. 5.

The CELP coding circuit 32 is the same as the CELP coding circuit described before in connection with Fig. 2 except for the operation of the multi-pulse retrieving circuit. For this reason,
5 only the operation of the multi-pulse retrieving circuit 401 will be described.

The multi-pulse retrieving circuit, designated at 401 in Fig. 5, generates the multi-pulse signal $C_j(n)$ on the basis of the pulse number P and $M(p)$
10 pulse position candidates of each pulse, set by the multi-pulse generation parameter setting circuit 33 and supplied through an input terminal 217, and selects a multi-pulse signal $C_j(n)$ that minimizes formula (4) noted above. As described before, in
15 the minimization of formula (4) the computational effort extent can be reduced by using the manner described in Literature 6.

The multi-pulse retrieving circuit 401 provides the selected multi-pulse signal $C_j(n)$ and reproduced
20 signal $SC_j(n)$ thereof to the gain retrieving circuit 211 and also provides corresponding index j through the output terminal 216 to the multiplexer 13. As described before in connection with Fig. 1, the multiplexer 13 provides a bit stream.

25 Referring back to Fig. 4, in the speech decoder the bit stream is received by the demultiplexer 14. As described before in connection with Fig. 1, the demultiplexer 14 provides the bit rate and coding

delay data present in the bit stream header to the coding parameter control circuit 34, then extracts the indexes representing the quantized LSP, pitch and multi-pulse signal from the bit stream for each
5 frame, and provides the extracted indexes to the CELP decoding circuit 35.

The coding parameter setting circuit 34 executes an operation similar to that in the coding parameter control circuit 31, thus selecting the
10 control parameters and providing the same to the CELP decoding circuit 35.

The multi-pulse coding parameter setting circuit 36 executes an operation similar to that in the coding side multi-pulse generation parameter
15 setting circuit 33, thus computing the pulse number representing the multi-pulse excitation signal, pulse position candidate number of each pulse and position candidates thereof, and providing the computed data to the CELP decoding circuit 35.

20 The operation of the CELP decoding circuit 35 will now be described with reference also to Fig. 6.

The CELP decoding circuit 35 is the same as the CELP decoding circuit described before in connection with Fig. 3 except for the operation of the
25 multi-pulse decoding circuit. For this reason, only the operation of the multi-pulse decoding circuit 402 will be described.

The multi-pulse decoding circuit, designated at

402 in Fig. 6, receives the sub-frame length set by the coding parameter control circuit 34 through the input terminal 229, receives the pulse number, pulse position candidate number of each pulse and position candidates thereof set by the multi-pulse coding parameter setting circuit 36 through an input terminal 232, and restores the multi-pulse signal by decoding from the indexes supplied for each sub-frame.

10 A further embodiment of the speech coder according to the present invention will now be described with reference to Fig. 7.

 The illustrated speech coder includes a coding parameter control circuit 61, a CELP coding circuit 62 and a multiplexer 13. The coding parameter control circuit 61 executes an operation similar to that in the coding parameter control circuit 11 described before in connection with Fig. 1, thus setting the frame length, sub-frame length and bit distribution from the supplied bit rate and coding delay data. The coding parameter control circuit 61 computes permissible multi-pulse signal coding computational effort extent, to which computational effort can be paid for the multi-pulse signal coding, from the supplied computational effort extent data. This computation can be executed by storing in advance data of computational effort extents necessary for the coding of other parameters

and subtracting these stored computational effort
extents from the supplied computational effort
extent. The coding parameter control circuit 61
provides frame length, sub-frame length, bit
5 distribution and permissible multi-pulse coding
computational effort extent as control parameters to
the CELP coding circuit 62.

The CDLP coding circuit 62 codes the input
signal on the basis of the supplied frame length,
10 sub-frame length, bit distribution and permissible
multi-pulse signal coding computational effort
extent data.

The operation of the CELP coding circuit 62
will now be described by having reference also to
15 Fig. 8.

The CELP coding circuit 62 is the same as the
CELP coding circuit described before in connection
with Fig. 2 except for the operation of the
multi-pulse retrieving circuit. For this reason,
20 only the multi-pulse retrieving circuit will be
described.

The multi-pulse retrieving circuit, designated
at 301 in Fig. 8, executes an operation similar to
that in the multi-pulse retrieving circuit 210
25 described before in connection with Fig. 2, thus
selecting a multi-pulse signal $C_j(n)$ that minimizes
formula (4) noted above. In this case, the
computational effort paid for the coding of the

multi-pulse signal, is preliminarily selected such that it does not exceed the permissible multi-pulse coding computational effort extent data supplied through an input terminal 218. This preliminary
5 selection can be realized by selection of a high value of $E1$ given by formula (9).

$$E1 = \left(\sum_{n=1}^L X(n) SCj(n) \right)^2 \quad (9)$$

10 The multi-pulse retrieving circuit 301 provides the selected multi-pulse signal $Cj(n)$ and reproduced signal $SCj(n)$ thereof to the gain retrieving circuit 211, and also provides corresponding index j through the output terminal 216 to the multiplexer 13.

15 A still further embodiment of the speech coder according to the present invention will now be described with reference to Fig. 9.

The illustrated speech coder includes a coding parameter control circuit 71, a multi-pulse
20 generation parameter setting circuit 33, a CELP coding circuit 72 and a multiplexer 13.

The coding parameter control circuit 71 executes an operation similar to that in the coding parameter control circuit 31 described before in
25 connection with Fig. 4, thus setting frame length, sub-frame length and bit distribution from the supplied bit rate and coding delay data. The coding parameter control circuit 71 computes permissible

multi-pulse signal coding computational effort
extent, which is paid for the coding of multi-pulse
signal, from the supplied computational effort
extent data. The coding parameter control circuit
5 71 provides the frame length, sub-frame length, bit
distribution and permissible multi-pulse signal
coding computational effort extent to the CELP
coding circuit 72. The coding parameter control
circuit 71 provides sub-frame length and bit number
10 distributed to the multi-pulse signal to the
multi-pulse generation parameter setting circuit 33.

The CELP coding circuit 72 codes the input
signal on the basis of the frame length, sub-frame
length, bit distribution and permissible multi-pulse
15 signal coding computational effort extent set by the
coding parameter setting circuit 71 and the pulse
number P , pulse position candidate number $M(p)$ of
each pulse and position candidates thereof set by
the multi-pulse signal generation parameter setting
20 circuit 33.

The operation of the CELP coding circuit 72
will now be described by having reference also to
Fig. 10.

The CELP coding circuit 72 is the same as the
25 CELP coding circuit described before in connection
with Fig. 5 except for the operation of the
multi-pulse retrieving circuit. For this reason,
only the operation for the multi-pulse retrieving

circuit 501 will be described.

The multi-pulse retrieving circuit, designated at 501 in Fig. 10, executes an operation similar to that in the multi-pulse retrieving circuit 401 described before in connection with Fig. 5, thus selecting a multi-pulse signal $C_j(n)$ that minimizes Formula (4) noted above. In this case, the computational effort paid for the coding of multi-pulse signal, is preliminarily set such that it does not exceed permissible multi-pulse signal coding computational effort extent supplied through an input terminal 218. The multi-pulse retrieving circuit 501 also provides the selected multi-pulse signal $C_j(n)$ and reproduced signal $SC_j(n)$ thereof to the gain retrieving circuit 211, and also provide corresponding index j through the output terminal 216 to the multiplexer 13.

As has been described in the foregoing, according to the present invention the frame length as a unit of processing for coding is made variable, permitting generation of parameters necessary for the coding of multi-pulse signal from given bit rate and coding delay data. Thus, it is possible to control not only the bit rate but also the coding delay and computational effort. According to the present invention, it is thus possible to use the same coder/decoder when it is desired to make the coding delay to be as short as possible for a

television conference system or the like or when it is desired to make the bit rate to be as low as possible rather than the coding delay for speech mail or like purposes. This permits scale reduction

5 of the coder/decoder.

Changes in construction will occur to those skilled in the art and various apparently different modifications and embodiments may be made without departing from the scope of the present invention.

10 The matter set forth in the foregoing description and accompanying drawings is offered by way of illustration only. It is therefore intended that the foregoing description be regarded as illustrative rather than limiting.